3. The system of claim 1 wherein two or more interrupts or exceptions may be mapped to one stream.

4. The system of claim 1 wherein mapping of interrupts to streams is static and determined at processor design.

5. The system of claim 1 wherein mapping of interrupts and exceptions is programmable.

6. The system of claim 5 wherein mapping is programmed in a data store, and the interrupt logic refers to the data store for mapping data to relate received interrupts or exceptions to streams.

7. The system of claim 1 wherein mapping is conditional and dynamic, the interrupt logic executing an algorithm sensitive to variables to determine the mapping.

8. The system of claim 1 wherein the interrupts are external interrupts generated by devices external to the processor.

9. The system of claim 1 wherein the interrupts are software interrupts generated by active streams.

10. The system of claim 6 wherein the data storage further comprises a mask for enabling/disabling execution of mapped interrupts or exceptions.

11. The system of claim 1 wherein, after mapping is determined for a detected interrupt or exception the one or more streams are interrupted by the interrupt logic.

12. The system of claim 11 wherein an interrupted stream acknowledges the interrupt, and is vectored to a service routing by the interrupt logic.

13. The system of claim 12 wherein two or more streams are interrupted by one interrupt or exception, and wherein the interrupt logic delays vectoring any stream to a service routine until all interrupted streams acknowledge the interrupt.

14. The system of claim 13 wherein two streams acknowledging the same interrupt are vectored to different service routines by the interrupt logic.

15. A method for processing interrupts in a multi-stream processor comprising steps of:

(a) detecting an interrupt or exception and passing the detected interrupt or exception to interrupt logic; and

(b) mapping the interrupt or exception to one or more streams of the multi-stream processor.

16 The method of claim 15 wherein, in step (b), the interrupt or exception may be mapped to two or more streams.

17. The method of claim 15 wherein, in step (a) two or more interrupts or exceptions are detected, and in step (b), the two or more interrupts or exceptions are mapped to one stream.

18. The method of claim 15 wherein mapping of interrupts to streams is static and determined at processor design.

19. The method of claim 15 wherein mapping of interrupts and exceptions is programmable.

20. The method of claim 19 wherein mapping is programmed in a data store, and the interrupt logic refers to the data store for mapping data to relate received interrupts or exceptions to streams.

21. The method of claim 15 wherein mapping is conditional and dynamic, the interrupt logic executing an algorithm sensitive to variables to determine the mapping.

22. The method of claim 15 wherein the interrupts are external interrupts generated by devices external to the processor.

23. The method of claim 15 wherein the interrupts are software interrupts generated by active streams.

24. The method of claim 20 wherein the data storage further comprises a mask for enabling/disabling execution of mapped interrupts or exceptions.

25. The method of claim 15 further comprising a step for, after mapping is determined for a detected interrupt or exception, the one or more streams are interrupted by the interrupt logic.

26. The method of claim 25 comprising a further step for vectoring an interrupted stream to a service routine after the interrupted stream acknowledges the interrupt.

27. The method of claim 26 wherein two or more streams are interrupted by one interrupt or exception, and wherein the interrupt logic delays vectoring any stream to a service routine until all interrupted streams acknowledge the interrupt.

28. The method of claim 27 wherein two streams acknowledging the same interrupt are vectored to different service routines by the interrupt logic.

29. A computing system comprising:

input apparatus for acquiring data to be processed;

memory elements for storing data and executable code for controlled use;

a multi-streaming processor having a plurality of streams for streaming one or more instruction threads; and

interrupt handling logic;

characterized in that through the interrupt logic specific interrupts or exceptions are detected and mapped to one or more specific streams.

30. The system of claim 28 wherein one interrupt or exception may be mapped to two or more streams.

31. The system of claim 28 wherein two or more interrupts or exceptions may be mapped to one stream.

32. The system of claim 28 wherein mapping of interrupts to streams is static and determined at processor design.

33. The system of claim 28 wherein mapping of interrupts and exceptions is programmable.

34. The system of claim 33 wherein mapping is programmed in a data store, and the interrupt logic refers to the data store for mapping data to relate received interrupts or exceptions to streams.

35. The system of claim 28 wherein mapping is conditional and dynamic, the interrupt logic executing an algorithm sensitive to variables to determine the mapping.

36. The system of claim 28 wherein the interrupts are external interrupts generated by devices external to the processor.

37. The system of claim 28 wherein the interrupts are software interrupts generated by active streams.

38. The system of claim 34 wherein the data storage further comprises a mask for enabling/disabling execution of mapped interrupts or exceptions.

39. The system of claim 28 wherein, after mapping is determined for a detected interrupt or exception the one or more streams are interrupted by the interrupt logic.

40. The system of claim 39 wherein an interrupted stream acknowledges the interrupt, and is vectored to a service routing by the interrupt logic.

41. The system of claim 40 wherein two or more streams are interrupted by one interrupt or exception, and wherein the interrupt logic delays vectoring any stream to a service routine until all interrupted streams acknowledge the interrupt.

42. The system of claim 41 wherein two streams acknowledging the same interrupt are vectored to different service routines by the interrupt logic.